IN THE CLAIMS

Please amend the claims as set forth below in marked-up form:

1. (Original) A PLL circuit, comprising:

an oscillator for generating an oscillation frequency signal having a variable oscillation frequency;

a phase detection circuit for comparing the phases of the oscillation frequency signal of said oscillator and an input signal with each other and outputting, based on a result of the comparison, a first phase control signal for advancing the phase of the oscillation frequency signal of said oscillator or a second phase control signal for delaying the phase of the oscillation frequency signal of said oscillator;

a signal generation circuit for generating first and second signals having different phases from each other based on the oscillation frequency signal of said oscillator; and

a frequency detection circuit for fetching the first and second signals generated by said signal generation circuit in synchronism with the input signal for each period of the input signal, logically operating the fetched signals and signals having been fetched in the immediately preceding period and outputting, based on a result of the arithmetic operation, a first frequency control signal for raising the frequency of the oscillation frequency signal of said oscillator or a second frequency control signal for lowering the frequency of the oscillation frequency signal of said oscillator.

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2. (Original) A PLL circuit according to claim 1, wherein the first and second signals are clock signals.

3. (Currently Amended) A PLL circuit according to claim 2, wherein the phases of the first and second signals ~~is different~~ differ from each other by 90 degrees ~~from each other~~.

4. (Original) A PLL circuit according to claim 1, wherein said frequency detection circuit includes a first sampling circuit for fetching the first signal in synchronism with the input signal for each period of the input signal, a second sampling circuit for fetching the second signal in synchronism with the input signal for each period of the input signal, and a control logic circuit for storing the signals fetched by said first and second sampling circuits, logically